IN THE CLAIMS:

Please ADD claims 12 and 13, as follows.

1-7. (Cancelled)

8. (Previously Presented) A method for manufacturing a semiconductor apparatus device including a plurality of layers on a semiconductor substrate, said method comprising the steps of:

dividing a pattern of at least a layer into a plurality of sub-patterns; and

joining the divided sub-patterns to perform patterning,

wherein as to a layer including wiring substantially affecting operation of the semiconductor device depending on a positional relationship to any other wiring, the patterning is performed by one-shot exposure using a single mask,

wherein only as to the layer including the wiring substantially affecting the operation of the semiconductor device depending on the positional relationship to any other wiring, the patterning is performed by one-shot exposure, and as to all of the other layers, the patterning is performed by division exposure.

9. (Previously Presented) A method for manufacturing a semiconductor apparatus device including a plurality of layers on a semiconductor substrate, said method comprising the steps of:

dividing a pattern of at least a layer into a plurality of sub-patterns; and

joining the divided sub-patterns to perform patterning,

wherein as to a layer including wiring substantially affecting operation of the semiconductor device depending on a positional relationship to any other wiring, the patterning is performed by one-shot exposure using a single mask,

wherein as to layers to be patterned prior to the patterning of the layer including the wiring substantially affecting the operation of the semiconductor device depending on positional relationship to any other wiring, the patterning is performed by one-shot exposure, and as to all of the other layers to be patterned after the one-shot exposure, the patterning is performed by division exposure.

10-11. (Cancelled)

12. (New) A method for manufacturing a semiconductor apparatus device, said method including the steps of dividing a pattern of at least one layer into a plurality of sub-patterns, and joining the divided sub-patterns to perform patterning, said method comprising the steps of:

forming source and drain regions of a MOS transistor on a semiconductor substrate;

forming a gate insulating film and a gate electrode of the MOS transistor;

forming a wiring layer including gate wiring connected to the gate electrode;

forming the gate wiring by performing patterning by means of a one-shot exposure to the wiring layer;

forming an insulating film after forming the gate wiring; and

forming a contact ~~hall~~ hole in the insulating film by using the steps of dividing a pattern of at least one layer into a plurality of sub-patterns, and joining the divided sub-patterns to perform patterning.

13. (New) The method according to claim 12, said method further comprising the step of forming a photoelectric conversion portion.